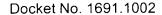


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## IN THE SPECIFICATION:

The specification as amended below with replacement paragraphs shows added text with <u>underlining</u> and deleted text with <u>strikethrough</u>.

Please REPLACE the paragraph beginning at page 3, line 7, with the following paragraph:

Conveniently the design verification process comprises, in a step prior to the determination of a reduced width RTL model, of determining the design specification of the digital circuit design and the specification of the properties to be investigated, synthesising synthesizing an RTL netlist of high level primitives, whereby the circuit is defined as an interconnection of control and data path portions, wherein signals of a width n are determined such that  $n \in \mathbb{N}_+$   $\frac{1}{12}$  wherein bitvectors of respective length determine the signal value and  $\mathbb{N}_+$  represents the natural numbers (excluding 0), i.e., 1, 2, 3, ... Conveniently, in the property checking process, an internal bit level representation contains a bit level variable for each bit of each word signal. This bit-level representation is passed to a verification engine and then to a property test unit which operates to provide a positive result if the investigated property holds true for the circuit and which operates to provide a counter-example if the property does not hold. In the event that a counter-example is produced for the reduced RTL design, signal width enhancement is performed to create a counter-example for the original RTL.